MULTISENSOR IMAGING SYSTEM VIDEO INTERFACE IMPLEMENTATION IN FPGA

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Abstract:
In this paper we describe practical implementation of FPGA based solution for converting signal from cameras with HD-SDI, analogue and camera link interfaces to common HDMI format. Main challenges like: frame rate equalization, image resolution adaptation and acts in case of camera connection loss are described in details. As a practical example we gave details about system with HD-SDI visible light camera, HD MWIR camera and analogue SWIR camera. In order to achieve target visibility in different day/night and meteorological conditions a multi-sensor imaging system combines signals from visible light camera, short wave infrared (SWIR) camera and medium (MWIR) or long (LWIR) wave infrared camera. Usually cameras originate from different vendor, with different interfaces, resolutions and frame rate. In order to enable further processing like image stabilization, enhancement, target tracking and image fusion, formats from all cameras should be converted to the same format.

Keywords:
Video, Multi-sensor, FPGA, Digital Signal Processing, Electro-Optical System.

1. INTRODUCTION

Multi-sensor imaging surveillance systems are under constant development and upgrade and have the large application in both civil and military defence [1]. The basic idea of Multi-sensor system is to combine data from different types of sensors (thermal sensors [2], colour cameras, low light cameras [3], SWIR cameras [4], laser range finders [5], etc.), process them for better situational awareness.

One example of multi-sensor system can be found in Figure 1, VMSIS3-C1200T [6] with courtesy of Vlatacom Institute. In most of these systems we can find a main multi-core CPU dedicated for Digital Video Signal Processing. It is usually a powerful hardware processor in which one can apply most of the Signal Processing Algorithms. Usually, the main CPU has to have unique video source input, but cameras originate from different vendors and have different types of interface, resolution and frame rate.

Our approach is to achieve a unified interfacing solution and implement it on an FPGA [7] architecture to convert any kind of input camera

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DOI: 10.15308/Sinteza-2019-561-566

interface to common HDMI [8] interface of any resolution and frame rate, according to input camera synchronization signals. In our particular case, it has also been developed a dedicated hardware platform which main parts are interface board, FPGA carrier board and main processor carrier board. For main processor we have decided to use Nvidia Jetson TX2 [9], which has a powerful hardware structure dedicated for Video Signal Processing. The main accent in this paper is on FPGA implementation for collecting video input data from interface board (with different types of connectors and interfaces) and converting that data into HDMI parallel data.

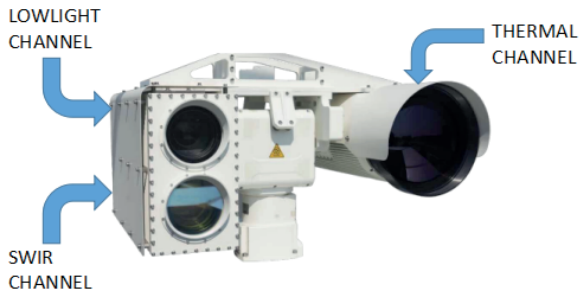

Figure 1. Multi-Sensor Imaging System - VMSIS3-C1200T

2. SYSTEM ARCHITECTURE

Entire system block design is shown in Figure 2. The main idea is to create a unified video signal processing platform which takes an input from various camera interface, prepares the data for main processor, which is in this case, NVIDIA Jetson TX2, and outputs the live stream via Ethernet interface. This applies for single channel camera streams.

For multi-sensor platform, these modules can be multiplied, with one main processor as a master channel, which controls the other channels. NVIDIA Jetson TX2 is capable to provide multiple stream views via Ethernet interface. The main operator PC should be used in this case with console application that sends and receive commands to/from master channel controller. All Video Signal Processing like image fusion, tracking, motion detection, pseudo-colouring, etc. Can be implemented on NVIDIA Jetson TX2, which is multicore platform with 256 parallel GPU CUDA [10] cores.

In the input stage, chipset for input pipeline is dedicated to convert data from any camera interface to parallel data that represents an input for FPGA processing. FPGA then converts input parallel data to HDMI parallel data and outputs it towards the output chipset pipeline which then converts this data into HDMI stream in first stage and to MIPI-CSI2 in the second stage. MIPI-CSI2 [11] lines are input for main Video Processing Unit (NVIDIA Jetson TX2).

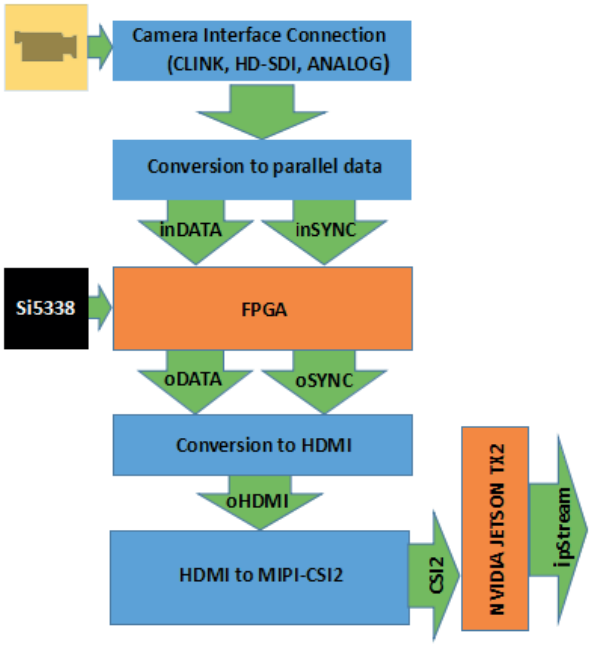

Figure 2. System Block Design

3. FPGA SIGNAL PROCESSING ARCHITECTURE

FPGA System Architecture is shown in Figure 3. The purpose of this design is to detect the presence of input camera, converts its format to appropriate format for the main CPU and outputs that format towards the CPU.

Signals from Camera interface are being converted to parallel data stream in the input stage pipeline and that represents the input for FPGA design. After the processing is done, the FPGA outputs processed data stream, according to HDMI standard towards the output pipeline, which converts parallel HDMI data to common HDMI video signal.

When Camera is present and powered on, the input stage pipeline delivers the parallel data from camera input interface. These parallel data can be divided into two sections:

- Synchronization signals (4 lines)
- Data signals (up to 24 lines)

Synchronization signals are Frame Valid, Line Valid, Data Valid and Pixel Clock. Those signals serve as an input to **Dual Port RAM** module. When Data Valid signal is active, pixel data from Data signals are been written to memory, synchronous to Camera Clock (Pixel Clock). When Frame Valid Signal is active, the Memory Address for writing data has been reset so the entire frame is written to Memory.

HDMI Driver module produces the four synchronization signals according to HDMI standard. Those signals are input for the reading side of the Dual Port RAM module. When Data Valid Signal is active, data is been read from Memory and outputted toward the main processor, synchronous to Camera Clock. When Frame Valid Signal is active, the read address has been reset, so that we read from beginning of the frame.

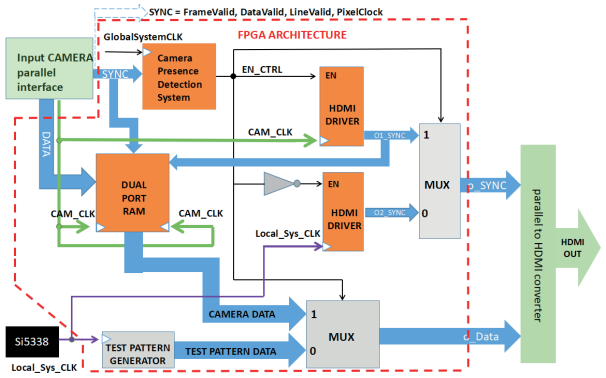

Figure 3. FPGA System Architecture

The **Camera Presence Detection System** module is designed to monitor the input synchronization signals from camera interface. If the synchronization signals are in expected values (defined by constants inside the module), the **Camera Presence Detection System** outputs a logical 1 and enables the HDMI Driver which is driven by Camera Clock, so the live stream from camera is outputted to main CPU. If the synchronization signals are not in expected values, the **Camera Presence Detection System** outputs a logical 0, which enables the HDMI Driver that is driven by Local System Clock and Test Pattern image is outputted to main CPU.

Test Pattern Generator is a VHDL module designed to output Greyscale pixel data driven by Local System Clock, so that, in case of absence or malfunction of camera, the test pattern image is streamed.

The FPGA projects for various input camera interfaces are designed to work in 3 different clock domains: Camera Clock (13.5 - 74.25MHz), Global System Clock (100MHz) and Local System Clock (13.5 - 74.25MHz) based on Si5338 IC [12], which configuration depends on input camera clock. Si5338 is a precise quad clock generator and it is configurable by I2C interface via main processor.

Camera Input Clock is used for live streaming picture from input camera.

Local System Clock is used to stream test pattern image when input camera is not plugged or malfunctioning.

Global System Clock is used to monitor all processes in project design and to trigger resynchronization between input and output image streams in case when switching from Test Pattern to live stream and vice versa.

4. PRACTICAL IMPLEMENTATION

For practical implementation, on Figures 4 and 5 we can see an example of design of printed circuit board (PCB) - an FPGA Carrier Board (FCB). On the figures below are displayed top and bottom layer design.

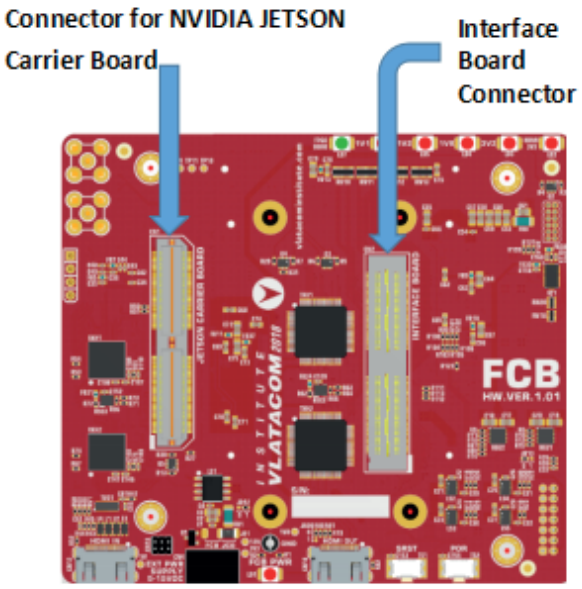

Figure 4. Top Layer View of PCB - FCB

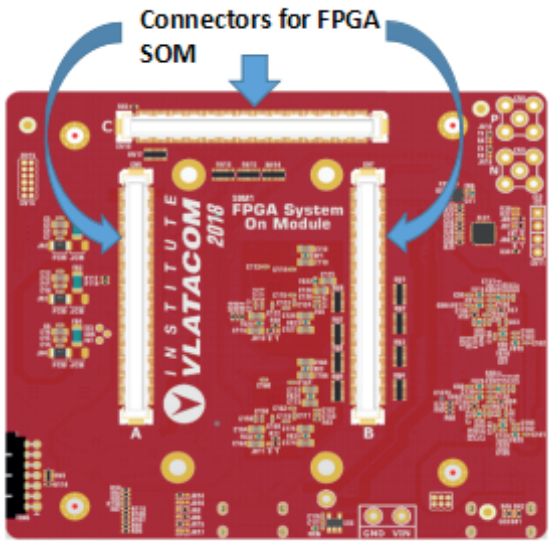

Figure 5. Bottom Layer View of PCB - FCB

As it is shown in the figures above, the PCB is designed to be modular, so it has a few connectors for interfacing a main processor board, camera interface boards (Camera Link [13], Analog [14], HD-SDI [15]) and FPGA System on Module (SOM). FPGA SOM and main processor board can be a custom board, according to requirements. Camera interface board is connected to FCB according to the input camera interface type and appropriate FPGA bitstream is downloaded to FPGA SOM.

For Multi-sensor imaging system shown on Figure 1, the described hardware is present on every channel. Characteristics of each channel and parameter settings can be seen in Table 1.

The parameters from table describe input camera sensor characteristics as well as some core settings for FPGA projects, for each camera. It is important to notice configuration for Local System Clock, which is configurable by I2C interface via main processor. For each channel there is a clock setting for transferring 30 frames per second or 60 frames per second, depending on project needs and applied video processing algorithms on main CPU. The Functional block design of Si5338 Clock generator can be found in Figure 6. The input internal oscillator has a base frequency of 24MHz.

As we can see in the Table 1, for Lowlight Channel size of FIFO buffer is quarter from full resolution. That is because in particular FPGA module there is not enough block RAMs for entire frame to store. Because of lack of memory resources, the synchronization between input and output Frame Valid signal is implemented, so we can read entire frame from beginning. This lack of memory can be avoided by adding one DDR4 external RAM module. FPGA used for this project is from Xilinx Kintex 7 Ultrascale plus series [16].

Table 1. Implemented version of fpga architecture in VMSIS3-C1200T

Resolution	1920x1080	720x576	1280x720
FPS	30/60	25/50	30/60
Data Type	YCbCr	YCbCr	RGB - Mono
Interface	HD-SDI	Analog	Camera Link
Scanning Type	Progressive	Interlaced	Progressive
Pixel Clock	74.25MHz	27MHz	74.25MHz
Local System Clock	37.125/74.25MHz	13.5/27MHz	37.125/74.25MHz
Global System Clock	100MHz	100MHz	100MHz
Dual Port RAM FIFO size	480x1080x20bit	720x576x20bit	1280x720x8bit
HDMI frame size	1920x1080	720x576	1280x720
HDMI extended frame size	2200x1125	864x625	1650x750

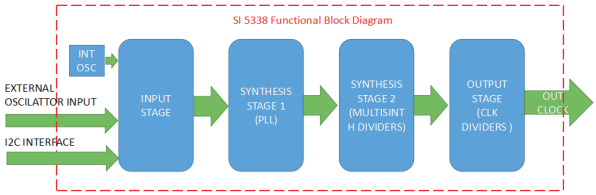

Figure 6. Functional Block Design of Si5338 Clock generator

Figure 7 shows a test pattern image displayed on live stream when camera is absent or malfunctioning.

The System was on the field test in Abu Dhabi, United Arab Emirates. The shown target, Hyatt Capitol Gate hotel was on the distance of 7.5 kilometres. Climate conditions were 43 degrees of Celsius outer temperature, sunny and clear.

Figures 8, 9 and 10 show a live stream from the system shown on figure 1, on all three channels: Low Light, SWIR and MWIR Thermal, respectively.

Figure 7. Test Pattern Live Stream

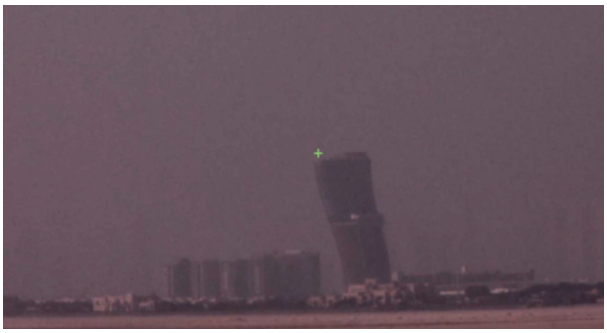

Figure 8. LowLight Channel Live Stream

Figure 9. SWIR Channel Live Stream

Figure 10. MWIR Thermal Channel Live Stream

5. CONCLUSION

The described and implemented unified solution for interfacing cameras with video processing units has proven to have a lot of advantages in comparison to most platforms currently available on the market. First of all is its modular design and reprogrammable hardware, so for any type of camera input interface, only the interface board should change. One interface board is present per one camera interface. Also, a hardware PCB is designed so that processing blocks can be easily changed (main signal processing processor and FPGA can be a matter of choice).

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